**PATENT** 

Attorney Docket No. MTI-31041-A

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Ping, et al.

Serial No.

10/046,497

Filing Date

October 26, 2001

For

Method For Forming Raised Structures by Controlled Selective

Epitaxial Growth of Facet Using Spacer

Group Art Unit

2814

Examiner

LE, Thao X.

Confirmation No.

8624

**FAX COPY RECEIVED** 

OCT 282002

CERTIFICATION UNDER 37 CFR 1.8(a) and 1.10

I hereby certify that, on the date shown below, this correspondence is being:

**TECHNOLOGY CENTER 2800** 

Mailing

deposited with the United States Postal Service in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

37 CFR 1.8(a)

37 CFR 1.10

□ with sufficient postage as first class mail □ As "Express Mail Post Office to Addressee" Mailing Label No.

Transmission

transmitted by facsimile to Fax No. (703) 308-7722 addressed to Examiner LE at the US Patent and Trademark Office

Date: 10-2808

Assistant Commissioner for Patents

Washington, D.C. 20231

## RESPONSE TO RESTRICTION REQUIREMENT

Sir:

In response to the Examiner's requirement for an election of species, mailed September 30, 2002, Applicant elects Subgroup "b", Figs. 24 with traverse.

Applicant traverses the Examiner requirement for election of species.

First, contrary to the Examiner's statement, Applicant submits that Claims 129, 143, 149, 173, 176, 179, 182, 186, and 190 are generic to all of Species a-c.

Serial No. 10/046,497

Response to Restriction

Second, Applicant respectfully disagrees with the identification of Species, and submits that the Examiner's characterization of the claims is in error.

The pending claims are not method claims.

Claims 101-128 recite a transistor.

Claims 129-181 recite a semiconductor structure.

Claims 182-193 recite a semiconductor device.

Each of the pending Claims 101-193 recite a structure comprising at least two overlying epitaxial layers having insulated sidewalls and an uppermost layer with an insulated top surface, or being covered by an insulative layer.

a transistor gate and/or a source/drain region with at least two Claims 101-116:

overlying layers of epitaxially grown silicon.

Claims 117-122: a transistor gate with multiple overlying epitaxial layers.

a source/drain region with at least two overlying layers of Claims 123-128:

epitaxially grown silicon.

a semiconductor structure or device with at least two overlying Claims 129-193:

layers of epitaxially grown silicon — which can be a transistor

gate, source drain region, or other structure.

The claims readable on Species "b" — illustrated in FIGS. 2D, 2E, 2F are Claims 101-116, 123-135, 137-160 and 165-193

It is also pointed out that the claims readable on the remaining species are as follows;

Species "a" — illustrated in FIG. 1H — Claims 110-115, 123-136, 140-156, 158-160, 169, 172, 173, 175, 176, 178-179, 181-183, 185-187, 189-191, and 193.

Species "c" — illustrated in FIG. 3C — Claims 117-122, 129-135, 138-139, 143-157, 161-168, 170-171, 173-174, 176-177, 179-180, 182-184, 186-188, and 190-192.

Serial No. 10/046,497

Response to Restriction

Applicant notes that the election of species is for the purpose of prosecution on the merits, and that Applicant will be entitled to consideration of claims to additional species upon allowance of a generic claim.

Applicant believes that the claims are in condition for allowance, and notification to that effect is respectfully requested.

Respectfully submitted,

Kristine M. Strodthoff
Registration No. 34,259

Dated: October 28 , 2002

DO LODDEGG

P.O. ADDRESS: WHYTE HIRSCHBOECK DUDEK S.C. 111 East Wisconsin Avenue, Suite 2100 Milwaukee, Wisconsin 53202 (414) 273-2100

Customer No. 022202

FAX COPY RECEIVED

OCT 28 2002

TECHNOLOGY CENTER 2800